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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/716,787	11/20/2000	Joseph Quinn Chapman	061606-1241	9842

24504 7590 08/26/2004

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EXAMINER

TORRES, JOSEPH D

ART UNIT	PAPER NUMBER
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2133

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DATE MAILED: 08/26/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/716,787

Applicant(s)

CHAPMAN, JOSEPH QUINN

Examiner

Joseph D. Torres

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 01 December 2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-79 is/are pending in the application.
- 4a) Of the above claim(s) 1-69 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 70-79 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☒ Claim(s) 1-69 are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 20 November 2000 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date 2.
- 4) ☒ Interview Summary (PTO-413)
Paper No(s)/Mail Date 2.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Restriction to one of the following inventions is required under 35 U.S.C. 121:
 - I. Claims 1-59, drawn to A digital subscriber line (DSL) communication device, comprising a digital signal processor (DSP) configured to perform layer two error detection in the receiver, classified in class 714, subclass 776.
 - II. Claims 60-69, drawn to a digital signal processor (DSP) configured to perform OSI layer one processing and configured to perform OSI layer two error detection wherein said layer two error detection occurs in the DSP, classified in class 714, subclass 776.
 - III. Claims 70-79, drawn to a digital signal processor (DSP) comprising layer one logic configured to perform OSI layer one processing and frame check sequence logic configured to compute a frame check sequence wherein the layer one logic has access to said frame check sequence, classified in class 714, subclass 774.

The inventions are distinct, each from the other because of the following reasons:

Inventions Group III and Group I are related as combination and subcombination.

Inventions in this relationship are distinct if it can be shown that (1) the combination as claimed does not require the particulars of the subcombination as claimed for

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patentability, and (2) that the subcombination has utility by itself or in other combinations (MPEP § 806.05(c)). In the instant case, the combination as claimed does not require the particulars of the subcombination as claimed because it does not require layer two error detection. The subcombination has separate utility such as for layer one error correction.

Inventions Group III and Group II are related as combination and subcombination.

Inventions in this relationship are distinct if it can be shown that (1) the combination as claimed does not require the particulars of the subcombination as claimed for patentability, and (2) that the subcombination has utility by itself or in other combinations (MPEP § 806.05(c)). In the instant case, the combination as claimed does not require the particulars of the subcombination as claimed because it does not require layer two error detection. The subcombination has separate utility such as for layer one error correction.

Because these inventions are distinct for the reasons given above and have acquired a separate status in the art as shown by their different classification, restriction for examination purposes as indicated is proper.

Because these inventions are distinct for the reasons given above and the search required for Groups I & II is not required for Group III, restriction for examination purposes as indicated is proper.

Because these inventions are distinct for the reasons given above and the search required for Group III is not required for Groups I & II, restriction for examination purposes as indicated is proper.

Because these inventions are distinct for the reasons given above and have acquired a separate status in the art because of their recognized divergent subject matter, restriction for examination purposes as indicated is proper.

During a telephone conversation with Karen Hazzah on 11 August 2004 a provisional election was made without traverse to prosecute the invention of Group III, claims 70-79. Affirmation of this election must be made by applicant in replying to this Office action. Claims 1-69 are withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention.

Drawings

2. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(4) because reference character "151" in Figure 4A has been used to designate both a data bus and a subtracter. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the

changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference character(s) not mentioned in the description: '24' in Figure 2; '36', '64' and '66' in Figure 3; '36', '112', '137', '154' and '156' in Figure 4A; '162', '181', '184' and '189' in Figure 4B; and '216' in Figure 6. Corrected drawing sheets in compliance with 37 CFR 1.121(d), or amendment to the specification to add the reference character(s) in the description in compliance with 37 CFR 1.121(b) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claim 71, 73, 76 and 78 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 71 recites the limitation "the adaptive parameters" in line 2. There is insufficient antecedent basis for this limitation in the claim.

Claim 73 recites the limitation "the adaptive parameters" in line 2. There is insufficient antecedent basis for this limitation in the claim.

Claim 76 recites the limitation "the adaptive parameters" in line 2. There is insufficient antecedent basis for this limitation in the claim.

Claim 78 recites the limitation "the adaptive parameters" in line 2. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 70 and 75 are rejected under 35 U.S.C. 102(b) as being anticipated by Byers; Larry L. et al. (US 5524218 A, hereafter referred to as Byers).

35 U.S.C. 102(b) rejection of claims 70 and 75.

Byers teaches a receiver for developing a received signal; and a digital signal processor

(DSP), where said DSP comprises: layer one logic configured to perform OSI layer one processing (col. 3, lines 26-32 in Byers teaches a first processor comprising a first physical layer controller for sending data packets over an optical fiber to a second processor comprising a second physical layer controller; Note: a packet transmitted over an optical fiber is a digital signal and since the first and second processors comprising first and second physical layer controllers are used for processing the packetized digital signal, the first and second processors comprising first and second physical layer controllers are digital signal processors; Note also: the physical layer is layer one of the Open System Interconnection networking architecture; hence said first and second DSP processors comprise: layer one logic, first and second physical layer controllers, configured to perform OSI layer one processing); and frame check sequence logic configured to compute a frame check sequence FCS on each frame of said received signal, wherein the layer one logic has access to said frame check sequence (col. 17, lines 29-39 in Byers teaches that the FCS is computed from a transmitted frame in a Physical Layer One control device; hence Byers teaches frame check sequence logic configured to compute a frame check sequence FCS on each frame of said received signal, wherein the physical layer one logic has access to said frame check sequence, since it is computed in a physical layer one device; Note: Frame Check Sequence operations are Data Link layer two operations, hence Byers teaches physical layer one processing of the Data Link layer two FCS, that is; Byers teaches performing, in the DSP, OSI layer one processing using the Data Link layer two frame check sequence).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
 2. Ascertaining the differences between the prior art and the claims at issue.
 3. Resolving the level of ordinary skill in the pertinent art.
 4. Considering objective evidence present in the application indicating obviousness or nonobviousness.
5. Claims 71-74 and 76-79 are rejected under 35 U.S.C. 103(a) as being unpatentable over Byers; Larry L. et al. (US 5524218 A, hereafter referred to as Byers) in view of Aoyagi; Hidehito et al. (US 4613975 A, hereafter referred to as Aoyagi).

35 U.S.C. 103(a) rejection of claims 71-74 and 76-79.

Byers substantially teaches the claimed invention described in claim 70 (as rejected above).

However Byers does not explicitly teach the specific use of saving adaptive parameters of an adaptive device located within said receiver, and calculated by said DSP, if said frame check sequence indicates that said received signal is error free.

Aoyagi, in an analogous art, teaches an error correction means using a comparator to supervise correction of tap coefficients for an equalizer (Note: and equalizer is a layer one device). The Abstract in Aoyagi teaches that coefficients are updated if the difference between reference data and the equalizer output exceed a threshold, i.e., if there are errors; hence if the threshold is not exceeded then the data is considered correct and coefficients are not updated. Note: coefficients are saved adaptive tap parameters for an equalizer of a receiver and an equalizer is a DSP or is part of a DSP; hence Aoyagi teaches saving adaptive tap coefficient parameters of an adaptive equalizer located within a receiver, and calculated by said DSP, if said frame check sequence indicates that said received signal is error free, that is; if the difference between a reference data and the equalizer output is small.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Byers with the teachings of Aoyagi by including use of saving adaptive parameters of an adaptive device located within said receiver, and calculated by said DSP, if said frame check sequence indicates that said received signal is error free. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that use of saving adaptive parameters of an adaptive device located within said receiver, and calculated by said DSP, if said frame check sequence indicates that said received signal is error free would have provided the opportunity to adjust tap coefficients of a receiver's equalizer to improve reception.

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

6. Claims 70-79 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 6-14 of U.S. Patent No. US 6272108 B1 in view of Aoyagi; Hidehito et al. (US 4613975 A, hereafter referred to as Aoyagi).

Claim 6 of .S. Patent No. US 6272108 B1 teaches method for updating adaptive parameters in a digital subscriber line (DSL) communication device, comprising the steps of: developing, in a receiver, a received signal; and performing, in a digital signal processor (DSP), layer two error detection by computing a frame check sequence (FCS) on each frame of said received signal, wherein said step of performing layer two error detection occurs in layer one of the OSI seven layer model.

However claim 6 of .S. Patent No. US 6272108 B1 does not explicitly teach the specific use of saving adaptive parameters of an adaptive device located within said receiver,

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and calculated by said DSP, if said frame check sequence indicates that said received signal is error free.

Aoyagi, in an analogous art, teaches an error correction means using a comparator to supervise correction of tap coefficients for an equalizer (Note: and equalizer is a layer one device). The Abstract in Aoyagi teaches that coefficients are updated if the difference between reference data and the equalizer output exceed a threshold, i.e., if there are errors; hence if the threshold is not exceeded then the data is considered correct and coefficients are not updated. Note: coefficients are saved adaptive tap parameters for an equalizer of a receiver and an equalizer is a DSP or is part of a DSP; hence Aoyagi teaches saving adaptive tap coefficient parameters of an adaptive equalizer located within a receiver, and calculated by said DSP, if said frame check sequence indicates that said received signal is error free, that is; if the difference between a reference data and the equalizer output is small.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify claim 6 of .S. Patent No. US 6272108 B1 with the teachings of Aoyagi by including use of saving adaptive parameters of an adaptive device located within said receiver, and calculated by said DSP, if said frame check sequence indicates that said received signal is error free. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that use of saving adaptive parameters of an adaptive device located within said receiver, and calculated by said DSP, if said frame check sequence indicates that said received signal is error

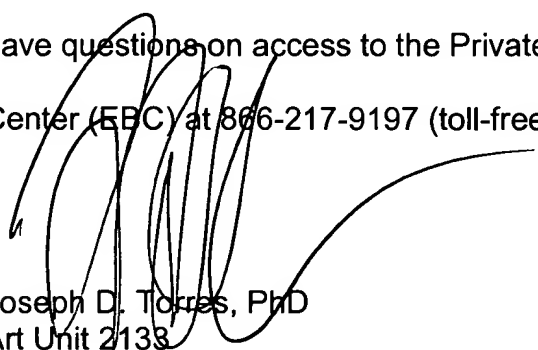
free would have provided the opportunity to adjust tap coefficients of a receiver's equalizer to improve reception.

Conclusion

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joseph D. Torres whose telephone number is (703) 308-7066. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (703) 305-9595. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Joseph D. Torres, PhD
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